WHAT WE CLAIM ARE:

1. A semiconductor device comprising:

a substrate comprising a first semiconductor and having a principal surface;

a plurality of quantum dots distributed dispersedly on the principal surface;

a cover layer comprising a second semiconductor and formed on a plane on which said quantum dots are distributed; and

a barrier layer comprising an insulator or a third semiconductor having a band gap wider than band gaps of the first and second semiconductors and disposed on the plane on which said quantum dots are distributed and at least in a partial area of an area not disposed with said quantum dots.

2. A semiconductor device according to claim 1, further comprising:

a quantum well layer comprising a fourth semiconductor having a band gap narrower than band gaps of the first and second semiconductors and disposed between the principal surface and the plane on which said quantum dots are distributed or between the plane on which said quantum dots are distributed and said cover layer; and

a tunneling layer disposed between said quantum well layer and the plane on which said quantum dots are distributed and having a thickness capable of serving as a potential barrier for energy levels in said quantum well layer and said quantum dots and allowing carriers to move between said quantum well layer and said quantum dots by a tunneling phenomenon.

3. A semiconductor device according to claim 2, wherein a composition and a

thickness of said quantum well layer and a composition and a size of each of said quantum dots are selected so that carriers can move from an energy level in said quantum well layer to an energy level in each of said quantum dots by a resonance tunneling phenomenon.

4. A semiconductor device according to claim 1, wherein said quantum dots comprise InGaAs and said barrier layer comprises material obtained by oxidizing Al-containing compound semiconductor.

5. A semiconductor device according to claim 1, wherein said cover layer is a single crystal layer epitaxially grown by inheriting crystallinity of the principal surface of said substrate.

6. A method of manufacturing a semiconductor device, comprising the steps of:

forming quantum dots distributed dispersedly on a principal surface of semiconductor;

forming a first layer comprising Al-containing compound semiconductor on the principal surface in an area not disposed with the quantum dots;

covering the quantum dots and the first layer with a second layer comprising semiconductor;

exposing side faces of the first layer; and

oxidizing the first layer from the exposed side faces.

7. A method of manufacturing a semiconductor device according to claim 6, wherein the quantum dots comprise InGaAs.

8. A semiconductor laser device comprising:

a substrate comprising first semiconductor of a first conductivity type;

a first separation confinement hetero layer formed on a surface of said substrate;

a plurality of quantum dots distributed dispersedly on said first separation confinement hetero layer;

a second separation confinement hetero layer formed on a plane on which said quantum dots are distributed;

a barrier layer disposed between said first and second separation confinement hetero layers, on the plane on which said quantum dots are distributed and at least in a partial area of an area not disposed with said quantum dots, said barrier layer comprising insulator or semiconductor having a band gap wider than band gaps of said first and second separation confinement hetero layers;

a clad layer formed on said second separation confinement hetero layer and comprising semiconductor of a second conductivity type opposite to the first conductivity type; and

a pair of electrodes for applying a voltage existing between said substrate and said clad layer.

9. A semiconductor laser device according to claim 8, further comprising:

a quantum well layer disposed between the plane on which said quantum dots are distributed and said first separation confinement hetero layer or between the plane on which said quantum dots are distributed and said second separation confinement hetero layer, said quantum well layer comprising

semiconductor having a band gap narrower than band gaps of the first and second separation confinement hetero layers; and

a tunneling layer disposed between said quantum well layer and the plane on which said quantum dots are distributed and having a thickness capable of serving as a potential barrier for energy levels in said quantum well layer and said quantum dots and allowing carriers to move between said quantum well layer and said quantum dots by a tunneling phenomenon.